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EXAMINER
EISEN, ALEXANDER

ART UNIT	PAPER NUMBER
2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/778,761	ONOYA, SHIGERU
	Examiner	Art Unit
	Alexander Eisen	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2001 and 10 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 June 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Semiconductor Display Device and Method of Driving Semiconductor Display Device".

Drawings

3. The applicant has submitted corrected drawings in response to Notice To File Corrected Application Papers (paper #2 of 19 April 2001), FIGS. 16A-B (paper #3 of 27 June 2001). The examiner has approved the correction.

4. The following drawings are objected to because of minor informalities:

a. In FIG. 4, 2nd legend from top should read –period—instead of "pwriod".

b. In FIG. 6, 5th legend from top should probably read –fifth frame period—instead of the legend in foreign language.

c. In FIG. 8 the line connecting units 203 and 205 should be designated as –polarity data signal—instead "plarity data signal".

d. The legend designating an output from unit 206 in FIG. 8 is not in English language.

5. Figures 21A-D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. **Claims 1-7, 11-13, 15 and 18-20** are rejected under 35 U.S.C. 102(e) as being anticipated by **Cole, US Patent No. 6,469,684**.

With respect to **claims 1-4**, Cole discloses a method for driving an active matrix display device (AM-LCD 20 in FIG. 1A) comprising a plurality of pixels (sub-pixel 30 in FIG. 4A), each containing pixel TFT (52), a pixel electrode and opposing electrode (column 7, lines 44-60), and a liquid crystal formed between the plurality of pixel electrodes and the opposing electrode, wherein display signals (drive signals 40 in FIG. 4A) are inputted to the plurality of pixel electrodes through the plurality of pixel TFTs, wherein pixel signals inputted to the plurality of pixel electrodes have positive or negative polarity with the electrical potential of the opposing

electrode (common signal 56) as a standard, and wherein the pixel electrodes into which display signals having the positive polarity are inputted, and the pixel electrodes into which display signals having the negative polarity are inputted differ (change) every frame period (see FIG. 3 showing four consecutive frames and column 6, lines 21-40).

Regarding **claim 2**, Cole additionally teaches the switching of the plurality of pixel TFTs in accordance with a selection signal (50 in FIG. 4A and 118 in FIG. 5) inputted to the plurality of gate signal lines (column 7, lines 50-55).

As to **claim 3**, Cole in addition to discussion above teaches two methods of driving the display, frame-inversion method and column inversion method respectively (see FIG. 2A and FIG. 2C; column 4, lines 41-56; column 5, lines 21-28), wherein the display signals inputted to each of the plurality of source signal lines (40) always have the same polarity and wherein the pixel electrodes into which display signals having the positive polarity are inputted, and the pixel electrodes into which display signals having the negative polarity are inputted differ (change) every frame period.

As to **claim 4**, Cole teaches a row-inversion method of driving liquid crystal display (FIG. 2B, column 4, lines 57-63) wherein all source signal lines are driven with the same polarity within one line period, and wherein the pixel electrodes into which display signals having the positive polarity are inputted, and the pixel electrodes into which display signals having the negative polarity are inputted differ (change) every frame period.

With respect to **claims 5** and **15**, Cole teaches a random sequence pattern for inverting the polarities of the display signals inputted into the pixel electrodes every frame period (see FIG. 3 and column 5, lines 54-59).

As to **claims 6** and **18-20**, all the methods shown in FIGS. 2A-D cause the display signals inputted into the pixel electrodes to be inverted in two adjacent frame periods.

Regarding **claim 7**, Cole teaches a source signal line driver circuit (102); a gate signal line driver circuit (104); a plurality of source signal lines (116); a plurality of gate signal lines (118); a pixel portion (120); a display signal generation portion (see FIG. 5 and FIG. 6, includes clock 106 and frame sync 114 signals, D-flop 154, drive chain from drive data 130 to drive signal 150), wherein the pixel portion has a plurality of pixels (30), each containing pixel TFT (52) and a pixel electrode, wherein the display signal generation portion has a control portion (signals 130, 106, 158, 160, circuitry 154); a polarity data signal generation portion (drive signal sequence generator 152); a display signal selection portion (146, 148 and 150); an alternating polarity switching signal generating portion (XOR gate 156); a + side display signal generation portion and – side signal generation portion (146, 148; column 8, lines 58-67), which are selected by applying the alternating polarity switching signal from XOR gate 156 to the selection portion, wherein the polarity data signal generation portion inputs a polarity data signal into the alternating polarity switching signal generating portion, wherein the display signals are generated in the display signal selection portion from the image signals having a positive or negative polarity and the alternating polarity switching signal and are outputted into the source signal driver circuit (from driver buffer 150), wherein the display signals are sampled and inputted to the plurality of source signal lines (column 8, line 19-26), and wherein pixel signals inputted to the plurality of pixel electrodes have positive or negative polarity with the electrical potential of the opposing electrode as a standard, and wherein the pixel electrodes into which display signals

having the positive polarity are inputted, and the pixel electrodes into which display signals having the negative polarity are inputted differ every frame period.

As to **claim 11**, the polarity data, the data pattern generated by Cole sequence generator 152, comprises information regarding the polarity of the display signals inputted to all of the pixels and controls the selection of the polarity of drive signals (column 8, lines 64-67).

In regard to **claim 12,** Cole discloses a method (see also discussion related to claims 1-4 and claim 2 above) for driving an active matrix display device comprising a plurality of pixels, each containing pixel TFT, a pixel electrode and opposing electrode, and a liquid crystal formed between the plurality of pixel electrodes and the opposing electrode, wherein switching of the plurality of pixel TFTs is controlled in accordance with a selection signal, wherein display signals are inputted to the plurality of pixel electrodes through the plurality of pixel TFTs, wherein pixel signals inputted to the plurality of pixel electrodes have positive or negative polarity with the electrical potential of the opposing electrode as a standard, and wherein the display signals having the positive polarity are inputted to some of the plurality of the pixel electrodes, and the display signals having the negative polarity are inputted to other of the plurality of the pixel electrodes in first one frame period (see FIG. 3, Frame 1, for example), and wherein only some of the plurality of the pixel electrodes have the inverse polarity in second one frame period (see FIG. 3, Frame 2 and column 6, lines 24-28).

As to **claim 13,** see the discussion above relevant to claim 7 because claim 13 recites most elements of claim 7. In addition to that Cole teaches the limitations that has not been covered by that discussion, such as the elements cited in the last five lines of claim 13. Cole teaches the method of driving display device, wherein the display signals having the positive

polarity are inputted to some of the plurality of the pixel electrodes, and the display signals having the negative polarity are inputted to other of the plurality of the pixel electrodes in first one frame period (see FIG. 3, Frame 1 for example), and wherein only some of the plurality of the pixel electrodes have the inverse polarity in second one frame period (see FIG. 3, Frame 2 and column 6, lines 24-28).

8. **Claims 8** and **21** are rejected under 35 U.S.C. 102(b) as being anticipated by **Kanatani et al., ("Kanatani"), US 5,414,443.**

In regard to **claim 8**, Kanatani discloses a display device (a second embodiment is considered hereinafter for example) comprising a source signal driver circuit 2 (see FIG. 5 and details in FIG. 7); a gate signal line driver circuit 300; a plurality of source signal lines 102; a pixel portion 100; a gray scale voltage control portion 4 and a gray scale voltage power source (voltage signal supply 7); wherein the source signal line driver circuit has a D/A converter circuit (voltage selector 55 – see column 10, lines 26-32), wherein the pixel portion has a plurality of pixels, each containing a pixel TFT 104 and a pixel electrode 103, wherein the gray scale voltage control portion has a control portion 4, a polarity data signal generation portion 79 (see detailed voltage signal supply source in FIG. 7) and an alternating current signal generation portion 793-795, wherein the control portion controls driving of the polarity control portion, the source signal driver and the gate driver (see in FIG. 5 connections of the control portion 4 to the gate driver 300, source signal driver 2 and voltage signal supply 7). It should be noted here that a polarity data signal is simply a one-bit data that carries the information about polarity of a current line in a current frame. Kanatani employs the row (line) polarity inversion method, wherein for example in first one frame every odd-numbered horizontal line is of positive polarity and every even-

numbered line is of negative polarity, and in the following frame the polarity in each horizontal line is reversed. The polarity data signal is generated from sync signals using D-flops 791 and 792, then output through XOR gate 793. The alternating current generation portion can be identified in this embodiment as the output of the gate 793, which is connected via gates 795 and 794 with a positive and negative power source portions 70 and 74 to control the gray scale voltage of selected polarity that should be inputted into the D/A converter circuit (selector 55), in accordance with the alternating current signal (see column 11, line 21 – column 12, line 4). As a result the pixel electrodes to which the display signals having positive polarity are inputted and the pixel electrodes to which the display signals having negative polarity are inputted differ (change) every frame period (using row inversion method).

With respect to **claim 21,** a one-bit stream of data derived by the selector 79 and used to control the polarity of each line in every frame is representative of the polarity and therefore comprises the information regarding the polarity of the display signals inputted to all of the pixels via signal electrode 52 from the selector 55.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 9, 16, 17** and **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cole** in view of **Hasegawa et al.,** (hereinafter **Hasegawa), US 6,219,019.**

Claim 9 recites all the limitations of claim 7 and additional structural elements and their functions corresponding to a particular way of generating polarity data signal. These additional components are an address counter and a memory, wherein an address of the memory is specified in accordance with a counter signal outputted from the address counter and then polarity data signal generation portion inputs polarity data stored at specified address to the alternating current signal generation portion.

Cole discloses all the elements and their functions except for those identified in the above paragraph (see also the discussion related to claim 7 in the item 5).

Hasegawa teaches a method for driving a liquid crystal display including a polarity inversion controller 20 (FIG. 4), which employs a memory 60, wherein polarity data is stored (FIG. 10; column 19, lines 42-45), and an address counter 63, which specifies the address of the memory (column 19, lines 53-54).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Hasegawa in the display of Cole as an alternative design choice for generating polarity data, because Cole teaches various ways of creating the polarity inversion data patterns, including a pseudo-random one, wherein the sequence of the pattern is predetermined and therefore lends itself conveniently for incorporating it into a memory, so rather than generating that data "on the fly" as Cole does, it could be pre-generated and stored into a memory for further use with the same result as the Cole's. The advantage of using memory is that the function of the device can be easily re-programmed instead of re-designing the whole new circuitry.

As to **claims 16** and **17,** Cole teaches the method wherein the display signals inputted to each of the plurality of source signal lines always have the same polarity (column inversion method) as claim 3 requires, and the method wherein the polarity of all the display signals inputted to the plurality of source signal lines is the same polarity within one line (line inversion method) as claim 4 requires.

Cole does not explicitly teach, however, that random patterns can include random column inversion method or random line inversion method.

Hasegawa shows row (line) inversion method and column inversion method in FIGS. 7B and 7C respectively. The sequence includes four consecutive frames F1 through F4 showing that all the frames differ in polarity pattern. This sequence can be seen as "pseudo-random" switching of rows (lines) polarity (as in FIG. 7B) and "pseudo-random" switching of column polarity (as in FIG. 7C; column 16, lines 59-67). Hasegawa further teaches that in order to improve the quality of the display that employs an inversion method the lines for the inversion should be randomly selected (column 20, line 45-56).

It would be obvious to those skilled in the art to use the technique proposed by Hasegawa in the display of Cole, because both use the randomization method for polarity inversion in order to improve the quality of the image by removing unwanted artifacts, and the advantage of using row or column inversion methods in comparison with the methods wherein all pixels are randomly switched in polarity is in lesser memory requirements, since only information on the polarity of a whole line or row would be needed instead of that for each pixel.

As to **claim 22,** the polarity data generated by Cole sequence generator 152 (Cole) and data stored in the memory 63 (Hasegawa) both comprise information regarding the polarity of the display signals inputted to all of the pixels.

11. **Claims 10, 14** and **23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kanatani** in view of **Hasegawa**.

With respect to **claims 10** and **14** Kanatani discloses a display device comprising a source signal driver circuit 2 (see FIG. 5); a gate signal line driver circuit 300; a plurality of source signal lines 102; a pixel portion 100; a gray scale voltage control portion 4 and a gray scale voltage power source (voltage signal supply 7a); wherein the source signal line driver circuit has a D/A converter circuit (voltage selector 55 – see column 10, lines 26-32), wherein the pixel portion has a plurality of pixels, each containing a pixel TFT 104 and a pixel electrode 103, wherein the gray scale voltage control portion has a control portion 4, a polarity data signal generation portion 79 (see detailed voltage signal supply source in FIG. 7) and an alternating current signal generation portion 793-795, wherein the control portion controls driving of the polarity control portion, the source signal driver and the gate driver (see in FIG. 5 connections of the control portion 4 to the gate driver 300, source signal driver 2 and voltage signal supply 7). It should be noted here that a polarity data signal is simply a one-bit data that carries the information about polarity of a current line in a current frame. Kanatani uses the row polarity inversion method, wherein during one frame all odd-numbered horizontal lines are of positive polarity and all even-numbered lines are of negative polarity, and in the following frame the polarity in each horizontal line is reversed. The polarity data signal is generated from sync signals using D-flops 791 and 792, then output through XOR gate 793. The alternating current

generation portion can be identified in this embodiment as the output of he gate 793, which is connected via gates 795 and 794 with a positive and negative power source portions 70 and 74 to control the gray scale voltage of selected polarity that should be inputted into the D/A converter circuit (selector 55), in accordance with the alternating current signal (see column 11, line 21 – column 12, line 4).

Regarding **claim 10,** Kanatani does not disclose, however, the use of a counter and memory for controlling the polarity inversion, the polarity data is rather derived from the sync signals by the selector circuit 79.

Hasegawa teaches an alternative polarity inversion method for driving a liquid crystal display, which employs a memory 60 for storing polarity data (FIG. 10; column 19, lines 42-45), and an address counter 63, which specifies the address of the memory (column 19, lines 53-54). Hasegawa also teaches that disclosed method can be further improved by randomizing the polarity inversion for adjacent frames (column 20, lines 51-62) in order to eliminate the unwanted artifacts.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the polarity inversion controller suggested by Hasegawa in the display device of Kanatani, because this controller would allow to employ more sophisticated polarity inversion control, including randomization of a position in which the polarity inversion is effected, and thus to eliminate such artifact as the undesirable movement of that position being observed (column 20, lines 45-50).

As to **claim 14**, Kanatani does not discloses the polarity inversion method, wherein display signals having the positive polarity are inputted to some of the plurality of pixel

electrodes and display signals having the negative polarity are inputted to the other of the plurality of pixel electrodes in first one frame period, and wherein only some of the plurality of the pixels electrodes have the inverse polarity in second one frame period. Rather in Kanatani's method all the pixel electrodes invert the polarity in subsequent frame.

Hasegawa teaches a method of driving display device using line inversion technique, wherein lines in which the polarity inversion occurs can be randomly selected, thus leaving some lines wherein the polarity inversion is not executed for all pixel electrodes in the following frame, such as shown for example in FIGS. 12 and 17. FIGS. 7A-7F also illustrate different patterns for polarity inversion in four consecutive frames F1-F4, whereby not all the pixel electrodes undergo the polarity inversion from frame to frame.

It would have been obvious to those skilled in the art at the time of the invention to employ the randomization technique of Hasegawa in the display device of Kanatani, because this technique advantageously allows to eliminate the unwanted artifacts caused by regular sequential method in the polarity inversion scheme of the latter (see Hasegawa, column 20, lines 51-56).

As to **claim 23,** a one-bit stream of data derived by the selector 79 (Kanatani) and used to control the polarity of each line in every frame is representative of the polarity and therefore comprises the information regarding the polarity of the display signals inputted to all of the pixels. Also, data stored in the memory 63 (Hasegawa) comprises information regarding the polarity of the display signals inputted to all of the pixels.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamamoto et al., US 4,926,168, discloses a random setting for polarity reversal to eliminate crosstalks and display irregularity.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is **(703) 306-2988**. The examiner can normally be reached on M-F (9:00 a.m - 4:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on **(703) 305-4709**.

Any response to this action should be **mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or **faxed to:**

(703) 872-9314 (for Technology Center 2600 only).

Hand-delivered responses should be **brought to:** Crystal Park Two, 2121 Crystal Drive, Arlington, Virginia, Sixth Floor Receptionist.

Any inquiry of a general nature or relating to the status of this application or proceeding should be **directed to:** Technology Center 2600 Customer Service Office, whose telephone number is **(703) 306-0377**.

Alexander Eisen
January 11, 2003